a second conductive layer disposed below said first conductive layer the second conductive layer having a plurality of openings;

a third conductive layer disposed below said second conductive layer;

a first insulating interlayer disposed between said first conductive layer and said second conductive layer;

a first through hole provided in said first insulating interlayer;

a fourth conductive layer filling said first through hole;

a second insulating interlayer disposed between said second conductive layer and said third conductive layer;

a second through hole provided in said second insulating interlayer; and

a fifth conductive layer filling said second through hole, wherein said first insulating interlayer and said second insulating interlayer are connected to each other through said openings of said second conductive layer, and a contiguous section of said first insulating interlayer with said second insulating interlayer is, thereby, formed between said first conductive layer and said third conductive layer.

3. (Amended) The semiconductor device according to claim [1] 2, wherein said second conductive layer has a planar network pattern.

4. (Amended) [The semiconductor device according to claim 1] A semiconductor device having a multiple wiring layer structure, comprising:

a first conductive layer connected to a conductive member for external connection;

a second conductive layer disposed below said first conductive layer the second conductive layer having a plurality of openings;

a third conductive layer disposed below said second conductive layer;

a first insulating interlayer disposed between said first conductive layer and said second conductive layer;

a first through hole provided in said first insulating interlayer;

a fourth conductive layer filling said first through hole;

a second insulating interlayer disposed between said second conductive layer and said third conductive layer;

a second through hole provided in said second insulating interlayer; and

a fifth conductive layer filling said second through hole, wherein said first insulating interlayer and said second insulating interlayer are connected to each other through said openings of said second conductive layer, and a contiguous section of said first insulating interlayer with said second insulating interlayer is, thereby, formed between said first conductive layer and said third conductive layer, said third conductive layer is the lowest conductive layer formed on an insulating film covering a surface of a semiconductor substrate, and said third conductive layer is also provided with a plurality of openings.

6. (Amended) The semiconductor device according to claim [1] 2, wherein said conductive member for external connection is a bonding wire.

7. (Amended) The semiconductor device according to claim [1] 2, wherein said first conductive layer, said second conductive layer and said third conductive layer comprise aluminum as a major component, and said fourth conductive layer and said fifth conductive layer comprise tungsten as a major component.

8. (Amended) The semiconductor device according to claim [1] 2, wherein said semiconductor device further comprises an internal circuit, said internal circuit being formed by the multiple wiring layer structure, and said first conductive layer, said second conductive layer, said third conductive layer, said fourth conductive layer, said fifth conductive layer,

a3 said first insulating interlayer, said second insulating interlayer, said through holes, and said multiple wiring layer structure are formed by a collective production process.

12. (Amended) The semiconductor device according to claim [1] 2, wherein the first and second through holes are axially aligned.

13. (Amended) The semiconductor device according to claim [1] 2, wherein the first and second through holes are axially offset.

a4 14. (Amended) The semiconductor device according to claim [1] 2, wherein the fourth and fifth conductive layers do not overlap.

Please add claim 21 as follows:

a5 --21. The semiconductor device according to claim 4, wherein the contiguous section is formed perpendicularly between said first conductive layer and said third conductive layer.--

REMARKS

Claims 2-8, 12-14 and 21 are pending. By this Amendment, the title is amended, claims 1, 9-11 and 15-20 are canceled, claims 2 and 4 are placed in independent form, claims 3, 6-8 and 12-14 are amended to depend from claim 2, and claim 21 is added for clarity. No new matter is added.

The December 3 Office Action in the parent application rejects claims 2, 3, 6, 8, 13 and 14 under 35 U.S.C. §102(e) over Chittipeddi et al. (U.S. Patent No. 5,751,065).

Applicant submits that Chittipeddi et al. does not disclose or suggest that the first insulating interlayer and the second insulating interlayer are connected to each other through the openings of the second conductive layer, in a contiguous section of the first insulating interlayer with the second insulating interlayer is, thereby, formed between the first conductive layer and the third conductive layer, as recited in claim 2. In fact, as admitted by the Office Action, the openings 307 of the middle layer 215 are merely for stress relief, and